SAULT COLLEGE OF APPLIED ARTS & TECHNOLOGY

SAULT STE. MARIE, ONTARIO

COURSE OUTLINE

COURSE TITLE: INTERFACING

CODE NO.: CET 315-6

PROGRAM: ELECTRICAL & ELECTRONIC TECHNOLOGIST

SEMESTER: SIX

DATE: DECEMBER 24, 1987

TEACHING MASTER: PETER SAVICH

/ NEW _____ REVISION

APPROVED: L B Crozetti CHAIRPERSON 88/01/05 DATE

88.03.07

CET 315-6

INTERFACING

PHILOSOPHY / GOALS

THE OBJECTIVE OF THIS COURSE IS TO ENHANCE THE STUDENT'S KNOWLEDGE OF MICROPROCESSOR THEORY, PRACTICE AND APPLICATIONS, TOGETHER WITH REPRESENTATIVE PERIPHERAL DEVICES. THE PRIMARY MICROCOMPUTER SYSTEMS THAT WILL BE STUDIED IS THE IBM PC. THE PDP-11 COMPUTER SYSTEMS WILL ALSO BE EXAMINED. THE COURSE IS DESIGNED TO USE THE KNOWLEDGE AND EXPERIENCE OF ONE SYSTEM TO HELP IN THE TRAINING IN ANOTHER MICROCOMPUTER SYSTEM.

THE COURSE WILL PROVIDE A GENERAL KNOWLEDGE OF THE IBM PC ARCHITECTURE & OPERATING SYSTEM MS-DOS. THE MICROSOFT ASSEMBLY LANGUAGE WILL ALSO BE INVESTIGATED. THE MAT TRAINERS WILL PERMIT MEANINGFUL LAB EXPERIMENTS REQUIRING PERIPHERALS AND THE IBM PC TO BE INTERFACED.

THE ULTIMATE GOAL OF THIS COURSE IS TO PROVIDE AN ENVIRONMENT THAT ALLOWS THE PRACTICAL EXPERIENCE OF PROGRAMMING IN ASSEMBLY LANGUAGE AND HARDWIRING THE MICROCOMPUTER SYSTEMS FOR THE CONTROL OF SOME REPRESENTATIVE SYSTEM CONFIGURATIONS THAT WOULD BE REQUIRED TO BE MAINTAINED OR INSTALLED IN INDUSTRY BY THE GRADUATING TECHNICIAN OR TECHNOLOGIST.

METHOD OF ASSESSMENT

THE STUDENT WILL BE ASSESSED THROUGH A SERIES OF WRITTEN TEST (3), AND QUIZES

ALL QUIZES AND PRACTICAL DEMONSTRATIONS WILL BE GIVEN WITH - NO ADVANCE NOTICE.

ALL LAB ASSIGNMENTS WILL BE OF EQUIVALENT VALUE.

THE PERCENTAGE OF ASSESSMENT FOR TESTS AND LAB PROJECTS MAY VARY SLIGHTLY BUT ARE EXPECTED TO BE A 60/40 SPLIT.

COURSE GRADING SCHEME

1. TESTS

WRITTEN TESTS WILL BE CONDUCTED AS DEEMED NECESSARY. THEY WILL BE ANNOUNCED ABOUT ONE WEEK IN ADVANCE.

2. GRADING SCHEME

A+	90+	OUTSTANDING ACHEIVEMENT
A	80 - 89	ABOVE AVERAGE ACHEIVEMENT
B	70 - 79	AVERAGE ACHEIVEMENT
C	55 - 69	SATISFACTORY ACHEIVEMENT
U		UNSATISFACTORY GIVEN AT MIDTERM ONLY
S		SATISFACTORY GIVEN AT MIDTERM ONLY
R		REPEAT
X		A TEMPORARY GRADE THAT IS LIMITED TO INSTANCES WHERE SPECIAL CIRCUMSTANCES HAVE PREVENTED THE STUDENT FROM COMPLETING OBJECTIVES BY THE END OF THE SEMESTER. AN "X" GRADE MUST HAVE THE CHAIRPERSON'S APPROVAL AND HAS A MAXIMUM TIME LIMIT OF 120 DAYS.

3. UPGRADING OF INCOMPLETES

WHEN A STUDENT'S COURSE WORK IS INCOMPLETE OR FINAL GRADE IS BELOW 55%, THERE IS THE POSSIBILITY OF UPGRADING TO A PASS WHEN THE STUDENT'S PERFORMANCE WARRANTS IT. ATTENDANCE AND ASSIGNMENT COMPLETION WILL HAVE A BEARING ON WHETHER UPGRADING WILL BE ALLOWED. A FAILING GRADE ON ALL TESTS WILL REMOVE THE OPTION OF ANY UPGRADING AND AN "R" GRADE WILL RESULT. THE HIGHEST ON A RE-WRITTEN TEST OR ASSIGNMENT WILL BE 56%.

THE METHOD OF UPGRADING IS AT THE DISCRETION OF THE TEACHER AND MAY CONSIST OF ONE OR MORE OF THE FOLLOWING OPTIONS:

ASSIGNED MAKE-UP WORK
RE-DOING PROJECTS
RE-DOING OF TESTS
WRITTING OF COMPREHENSIVE SUPPLEMENTAL EXAMINATION

ADDITIONAL REQUIREMENTS

COMPLETION OF THE REQUIRED LAB PROJECTS IS NECESSARY FOR SUCCESS IN THIS COURSE. LATE SUBMISSION OF REPORTS AND POOR ATTENDANCE WILL HAVE A BEARING ON FINAL EVALUATION; GENERALLY , A LATE REPORT WILL BE GIVEN A "C" GRADE UNLESS EXTENUATING CIRCUMSTANCES ARE INVOLVED AND THE TEACHER IS INFORMED PRIOR TO THE SUBMISSION DEADLINE. THE SUCCESSFUL COMPLETION OF A MINIMUM OF THREE LAB PROJECTS IS NECESSARY.

LAB REPORT REQUIREMENTS

INFORMAL LAB REPORTS ARE DUE ONE WEEK AFTER COMPLETION AND WILL INCLUDE THE FOLLOWING:

1. TITLE PAGE
   INCLUDES: TITLE, DATE, LAB PARTNERS, PROJECT NO.

2. STATEMENT OF THE LAB'S OBJECTIVES

3. BRIEF STATEMENT OF THE PROCEDURE

4. CIRCUIT DIAGRAMS PROPERLY LABELLED

5. PROGRAM LISTINGS PROPERLY DOCUMENTED, DATA TABLES, TIMING DIAGRAMS, ETC.

6. WHERE ANY SPECIFIC QUESTIONS HAVE BEEN ASKED AS PART OF THE LAB PROCEDURE INCLUDE BOTH THE QUESTION AND ANSWER.

7. DISCUSSION OR CONCLUSION SECTION IN WHICH THE RESULTS ARE EVALUATED, DEFICIENCIES ARE DISCUSSED, AND DEGREE OF COMPLETENESS IS IDENTIFIED, AND THE IMPORTANT OBJECTIVES ARE SUMMARIZED.

WHEN A LAB GROUP WORKS ON A PROJECT TOGETHER, A SINGLE REPORT SHOWING CONTRIBUTIONS FROM BOTH MEMBERS WILL BE SUBMITTED. WHERE THE CONTRIBUTION OF ONE MEMBER OF A GROUP IS SEEN TO BE SIGNIFICANTLY LESS THAN ANOTHER, AS WOULD OCCUR FOR EXAMPLE, WHEN ONE MEMBER IS ABSENT FROM LAB SESSIONS, HE/SHE MAY NOT BE CREDITED WITH THE LAB PROJECT AND BE REQUIRED TO DO ANOTHER IN ITS PLACE.

TEXT BOOK:

1. "MICROCOMPUTER INTERFACING"

BY HAROLD S. STONE
ADDISON-WESLEY PUBL.

2. PDP-11

"MACRO-11 ASSEMBLY LANGUAGE ARCHITECTURE AND STRUCTURED PROGRAMMING"

BY C. J. HWANG, D.E. GIBSON
PRENTICE HALL PUBL.

3. IBM PC

"M.A.T. DOS FOR TECHNICIANS"

PREPARED BY E & L INSTRUMENTS

COURSE OUTLINE

* NOTE: THIS SET OF OBJECTIVES MAY REQUIRE SOME MODIFICATIONS AS THE SEMESTER PROGRESSES SINCE THIS IS A NEW COURSE. ANY REVISIONS TO THE OBJECTIVES WILL BE ISSUED BEFORE TESTS OCCUR.

BLOCK 1: MS DOS

AT THE END OF THIS BLOCK THE STUDENT SHALL BE ABLE TO:

1. CREATE, DELETE, RETRIEVE FILES AND DIRECTORIES

2. CREATE BATCH FILES AND USE THE BATCH PROCESSING COMMANDS

3. USE THE NORTON EDITOR TO EDIT FILES

4. USE THE MICROSOFT SYMDEB DEBUGGER AND THE IBM PC DEBUG

NOTE: THIS IS REVIEW AND UPGRADING FOR SOME OF THE STUDENTS AND COMPLETELY NEW MATERIAL FOR OTHERS IN THIS CLASS OFFERING OF THE COURSE.

BLOCK 2: ARCHITECTURE OF VARIOUS MICROPROCESSORS

THE STUDENT SHOULD BE ABLE TO:

1. DISCUSS THE EVOLUTION OF MICROPROCESSOR TECHNOLOGY

2. DISCUSS THE GENERAL ARCHITECTURE OF TYPICAL COMPUTERS.

3. DISCUSS THE FOLLOWING TOPICS:
   A) INTERNAL PROCESSOR ORGANIZATION
   B) DIFFERENCES BETWEEN SINGLE BUS SYSTEMS AND TWO PATH SYSTEMS
   C) THE GENERAL OPERATION OF THE DMA CONTROLLER
   D) DIFFERENCES BETWEEN PROGRAM CONTROLLED I/O AND INTERRUPT DRIVEN I/O CONTROL

4. DESCRIBE THE REQUIREMENTS OF AN INTERRUPT INTERFACE

BLOCK 3: SHEILDING AND GROUNDING CONCEPTS

THE STUDENT SHOULD BE ABLE TO:

1. DISCUSS THE NEED FOR SHEILDING OF COMPUTER CIRCUITRY

2. DESCRIBE TWO GENERAL RULES TO FOLLOW WHEN INTERCONNECTING COMPUTERS.

3. DESCRIBE THE TWO METHODS OF IMPROVING GROUNDING AND REDUCING CROSS-TALK IN FLAT CABLE.

4. DISCUSS TRANSMISSION LINE EFFECTS IN POINT-TO-POINT CONNECTIONS IN COMPUTER SYSTEMS AND BE ABLE TO DESCRIBE LINE TERMINATION TECHNIQUES TO MINIMIZE THESE EFFECTS.

BLOCK 4: COMPUTER BUSES

AT THE END OF THIS BLOCK THE STUDENT SHALL BE ABLE TO:

1. DESCRIBE THE NATURE OF A COMPUTER BUS AND ITS FUNCTIONS.

2. DESCRIBE THE VARIOUS BUS HANDSHAKES: ASYNCHRONOUS, SYNCHRONOUS, SEMI-SYNCHRONOUS

3. DESCRIBE THE THREE TYPES OF SIGNALS FOUND ON BUSES.

BLOCK 5: MEMORY SYSTEMS

AT THE END OF THIS BLOCK THE STUDENT SHALL BE ABLE TO:

1. DESCRIBE THE DIFFERENCE BETWEEN STATIC AND DYNAMIC RAM.

2. DESCRIBE THE CHARACTERISTICS OF ROM, PROM, EPROM AND BE ABLE TO DESIGN CIRCUIT APPLICATIONS USING THEM.

3. DESCRIBE THE TECHNICAL REQUIREMENTS FOR REFRESHING DYNAMIC RAM.

4. GIVEN CIRCUIT DIAGRAMS, DESCRIBE THE OPERATION AND ORGANIZATION OF THE IBM PC HARDWARE COMPONENTS:

	8284	CLOCK GENERATOR
PIC	8259	PROGRAMMABLE INTERRUPT CONTROLLER
PPI	8255	PROGRAMMABLE PERIPHERAL INTERFACE
PIT	8253	PROGRAMMABLE INTERVAL TIMER
	8288	BUS CONTROLLER

5. GIVEN THE MEMORY DESIGN OF THE IBM PC DISCUSS THE RAM ALLOCATION IN THE IBM PC, AND THE ROM ALLOCATION IN THE IBM PC

6. GIVEN CIRCUIT DIAGRAMS, DESCRIBE THE OPERATION AND ORGANIZATION OF THE M6800 16K MEMORY BOARD.

BLOCK 6: IEEE-488 BUS

THE STUDENT WILL DEMONSTRATE KNOWLEDGE OF THIS PARALLEL BUS INTERFACE BY BEING ABLE TO:

1. DISCUSS THE GENERAL CHARCTERISTICS OF PARALLEL PORT INTERFACES, AND THE OPEN COLLECTOR AND TRI-STATE DEVICES USED TO IMPLEMENT THEM.

2. DESCRIBE THE IEEE-488 BUS SIGNALS, AND THE PROTOCOL USED TO TRANSFER INFORMATION TO THIS BUS.

3. DESCRIBE THE OPERATION AND PROGRAMMING OF THE MC68488 INTEGRATED CIRCUIT.

BLOCK 7: MAGNETIC RECORDING

AT THE END OF THIS BLOCK THE STUDENT SHALL BE ABLE TO:

1. DESCRIBE THE VARIOUS METHODS OF ENCODING DIGITAL INFORMATION MAGNETICALLY ON DISKS AND TAPES.

2. GIVEN CIRCUIT DIAGRAMS, DESCRIBE THE OPERATION OF A FLOPPY DISK INTERFACE, AND A FLOPPY DISK DRIVE.

BLOCK 8: DISPLAY TECHNIQUES

AT THE END OF THIS BLOCK THE STUDENT SHALL BE ABLE TO:

1. DESCRIBE THE METHODS OF DISPLAYING DATA ON COLOUR AND BLACK AND WHITE CRT SCREENS.

2. DESCRIBE THE TYPICAL COMPONENTS OF A CRT DISPLAY INTERFACE.

3. DESCRIBE THE OPERATION OF THE MC6845 CRT CONTROLLER CHIP.

4. WRITE PROGRAMS TO INITIALIZE THE CRT CONTROLLER AND DISPLAY DATA ON THE CRT.

5. GIVEN CIRCUIT DIAGRAMS, DESCRIBE THE OPERATION OF THE D2 KIT CRT CONTROLLER BOARD.

POTENTIAL LAB ACTIVITIES:

LABS 1 AND 2 ARE MANDITORY FOR ALL PARTICIPANTS IN THE COURSE:

1. MS-DOS/ MAT TRAINERS / DEBUG / ASSEMBLER

2. USING THE D3 KITS WIREWRAP AND USE EPROM PROGRAMMER TO PUT THE PROGRAM THAT CONTROLS A MC6840 PROGRAMMABLE TIMER ON A 2716 EPROM.

   THIS PTM EXPERIMENT COULD BE REPLICATED USING THE HEATHKITS

LABS 3 THRU 7 ARE ADDITIONAL AND ARE ASSIGNED BY THE TEACHER TO THE STUDENTS. STUDENTS MAY INDICATE WHOM THEY PREFER TO WORK WITH AND WHICH PROJECTS THEY WOULD LIKE BUT THE DECISION RESTS WITH THE TEACHER AS TO PARTNERS AND LAB PROJECT.

3. USE THE D2 KIT 16K MEMORY EXPANSION BOARD / USE LOGIC ANALYZERS TO GENERATE TIMING DIAGRAMS FOR MEMORY REFRESH CYCLE

4. DEVELOP THE IEEE-488 PARALLEL BUS "ATE" SYSTEM FOR THE IBM PC OR PDP-11

5. USE THE D2 KIT AND THE 6845 CRT CONTROLLER BOARD

6. USE THE IBM-PC AND INTERFACE TO A WIRERAPPED A/D CONVERTOR

7. INTERFACE THE PDP-11 AND THE 6800 USING THE DIGITAL I/O